RS data

74 Series TTL
Standard, Low Power Schottky and Advanced Low Power Schottky

This data sheet gives pin connections and availability of the three TTL families offered.

Standard 74 series TTL

A range of popular transistor-transistor logic integrated circuits for use in cost effective circuits.

Low power schottky 74LS series TTL

A schottky process using shallower diffusions yields devices with a fivefold decrease in power consumption and an increase in speed compared to standard 74TTL.

Advanced low power schottky 74ALS series TTL

Advanced low power schottky TTL devices are directly compatible with LS and standard TTL devices. An advanced oxide isolated construction uses smaller geometries giving approximately twice the speed with half the power consumption of 74LS TTL.

Comparison of TTL, LS TTL and ALS TTL

	Speed/ Power Product	Propogation Delay	Power Dissipation	Clock Input Frequency Range
74 TTL	100 pJ	10ns	10mW	dc to 35MHz
74LS TTL	19 pJ	9.5ns	2mW	dc to 45 MHz
74ALS TTL	4 pJ	4ns	1mW	dc to 50MHz

All devices are designed to operate from a single 5 V dc supply and are housed in standard DIL plastic packages suitable for operation over the temperature range 0°C to + 70°C.

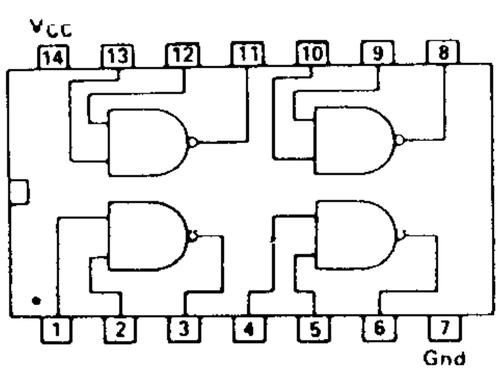
Theoretically, an unconnected input assumes a HIGH logic level, but practically it is in an undefined state because it acts as an antenna for noise. It is good design practice to connect unused inputs to the appropriate defined logic level in order to achieve output conditions in line with the device truth table. For active HIGH inputs with standard TTL and ALS TTL a pull-up resistor to Vcc should be used; up to 25 unused inputs can be connected to each resistor. With LS TTL, unused active HIGH inputs can be directly tied to Vcc so long as the connecting leads are short and the power supply is adequately decoupled. Unused active LOW inputs can be directly connected to ground with all families.

Connections shown are top view. A "negation" circle at any output or input within the schematic indicates that the terminal is active LOW or at clocking inputs the device is negative edge triggered.

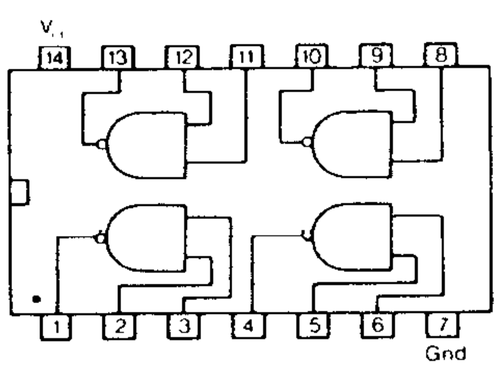
Abbreviations used throughtout this data sheet

A,B,C,D and E	Data inputs binary weight (where applicable) A = 1; B = 2; C − 4; D = 8; E = 16
a,b,c,d etc	Segment outputs on 7-segment decoder driver
BCD	Binary Coded Decimal
BI	Blanking Input
$C_{in,\ out}$	Carry in or out
CEP	Count Enable Parallel Input
CER	Count Enable Ripple Input
CK	Clock
CS	Clip select
D,JK	Data input to flip-flops
EN	Enable
GND	Ground OV terminal
I/O	Input/Output
LT	Lamp test
MR	Master Test
OEN	Output enable
PE	Parallel Enable (active low) Input
Q	Output, may have a letter indicating weighting
RBI	Ripple Blanking Input
RBO	Ripple Blankng Output
RC,C,R	Capacitor and Resistor timing on monostables
RCO	Ripple carry output
S	Sum Output
SDL	Serial data in Left Shift
SDR	Serial data in Right Shift
SQ	Serial Output
SR	Synchronous reset
TC	Terminal Count Output
V_{CC}	+ Supply terminal
	Schmitt Device or function

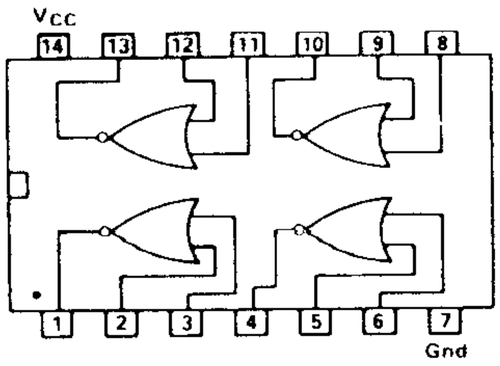
00 Quadruple 2-input NAND gate



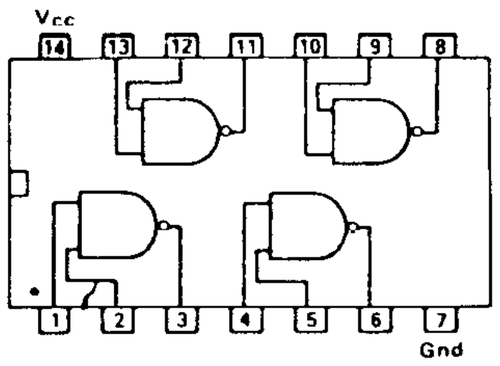
01 Quadruple 2-input NAND gate with open collector output



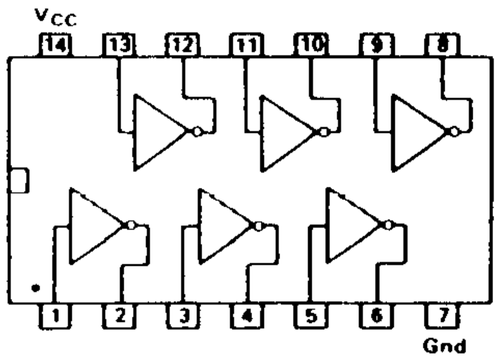
02 Quadruple 2-input NOR gate



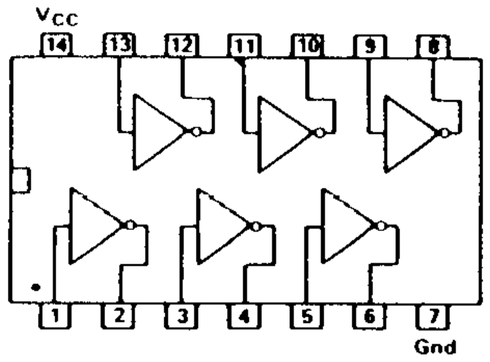
03 Quadruple 2-input NAND gate – open collector inputs



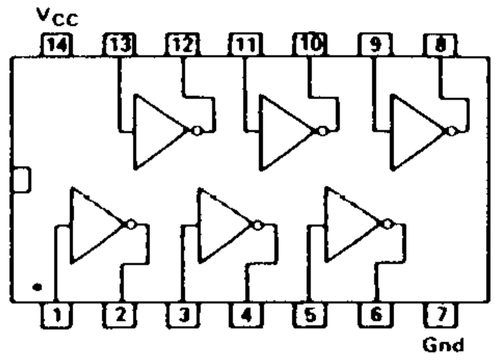
04 Hex inverter



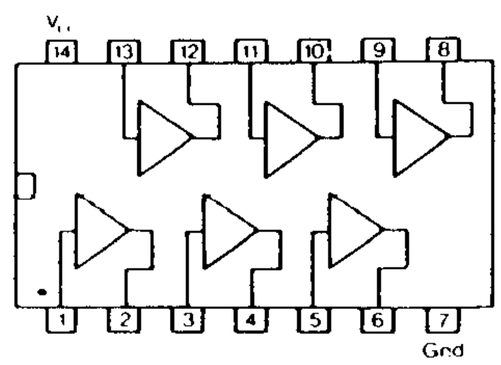
05 Hex inverter-open collector outputs



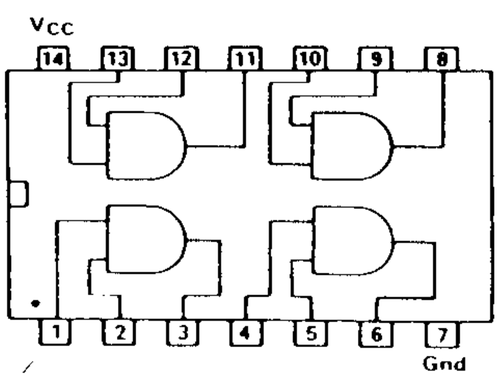
06 Hex inverter with high voltage open collector output



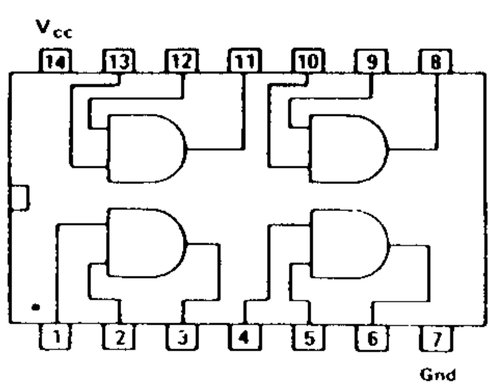
07 Hex driver with open collector output



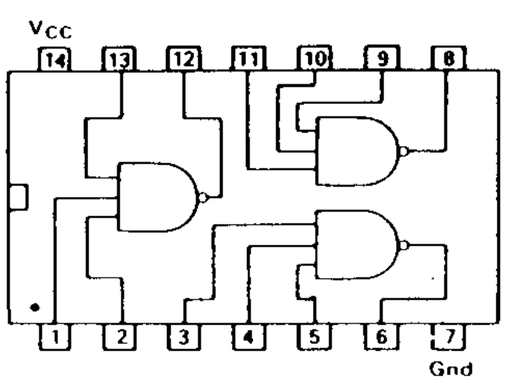
08 Quadruple 2-input AND gate



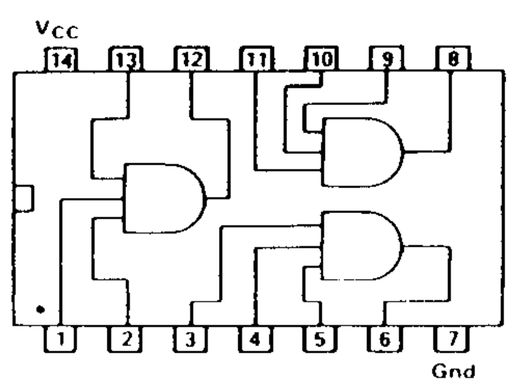
09 Quad 2-input AND gate-open collector outputs



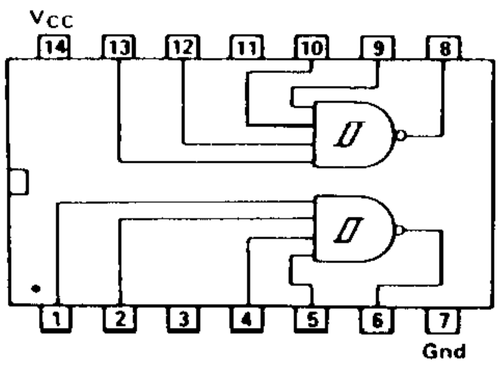
10 Triple 3-input NAND gate



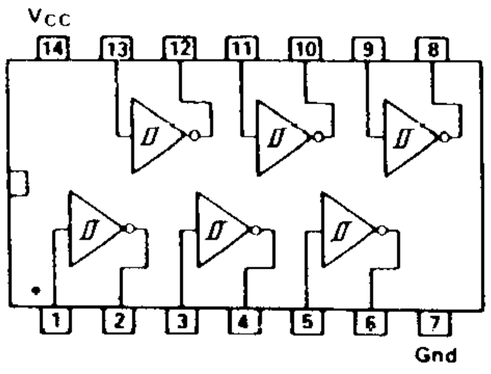
11 Triple 3-input AND gate



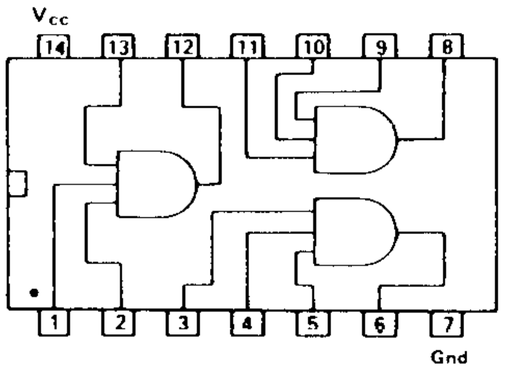
13 Dual 4 input NAND gate Schmitt trigger



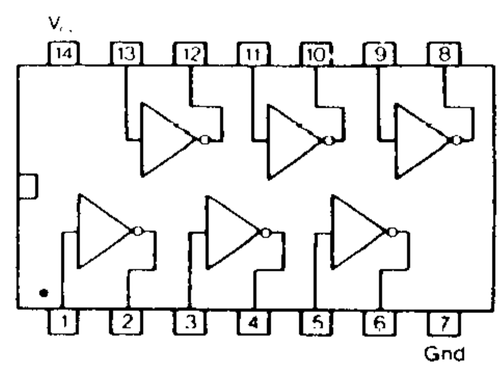
14 Hex Schmitt Trigger



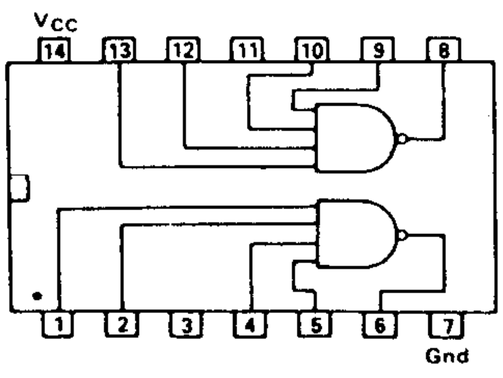
15 Triple 3 input AND gate – open collector outputs



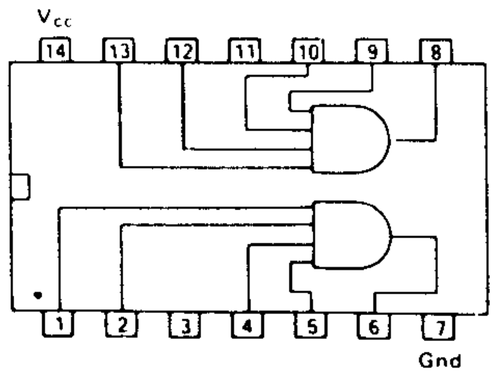
16 Hex Inverter with open collector output



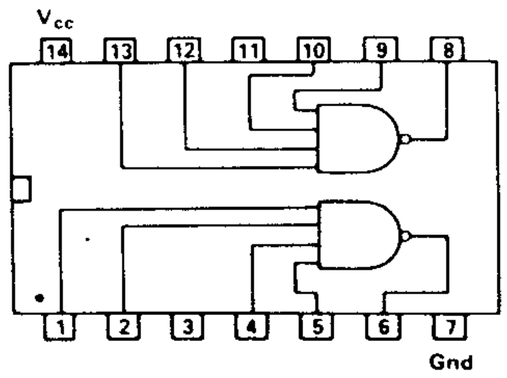
20 Dual 4-input NAND gate



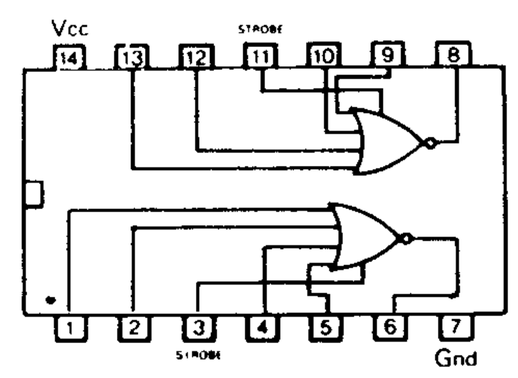
21 Dual 4-input AND gate



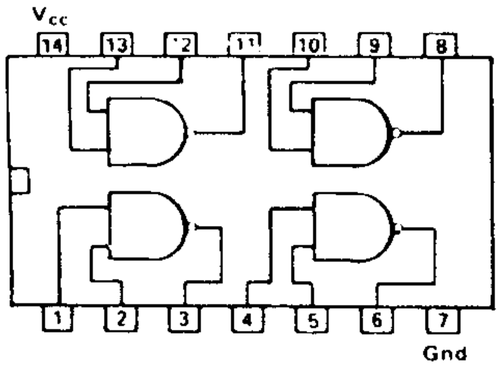
22 Dual 4-input NAND gate – open collector outputs



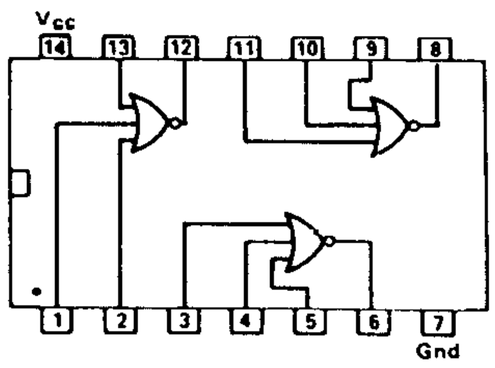
25 Dual 4-input NOR gate with strobe



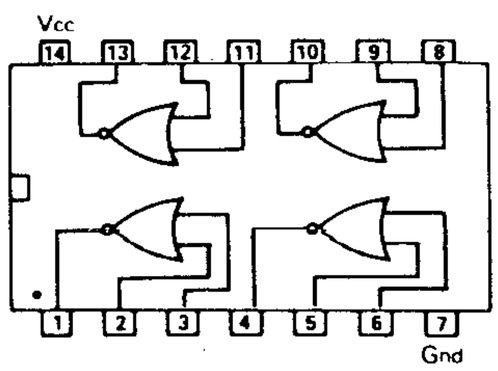
26 Quad 2-input NAND buffer-open collector outputs



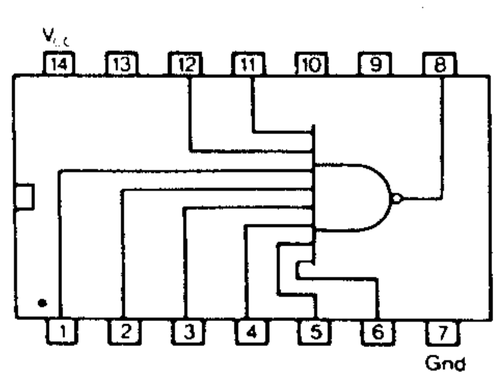
27 Triple 3-input NOR gate



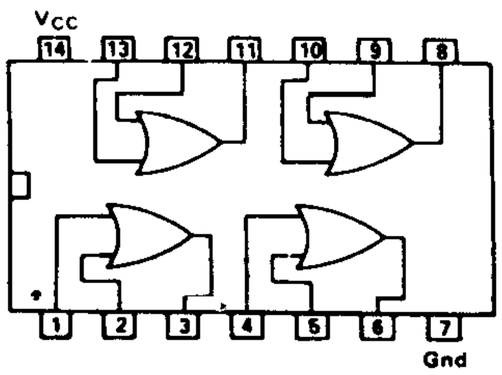
28 Quad 2-input NOR buffer



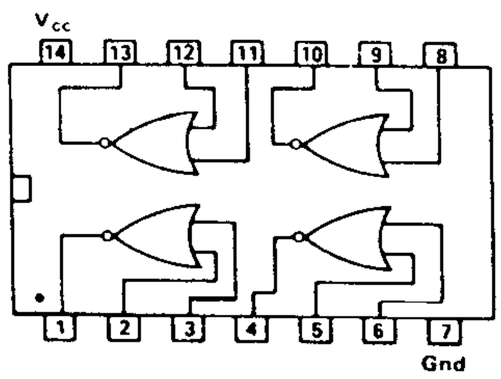
30 8-input NAND gate



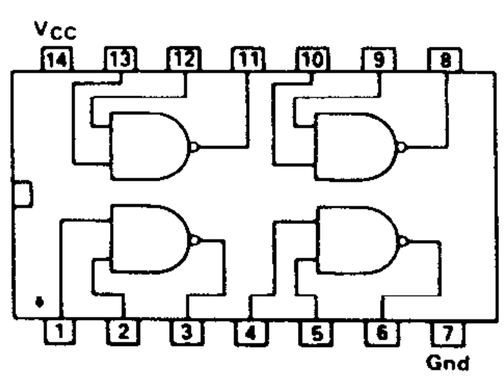
32 Quadruple 2-input OR gate



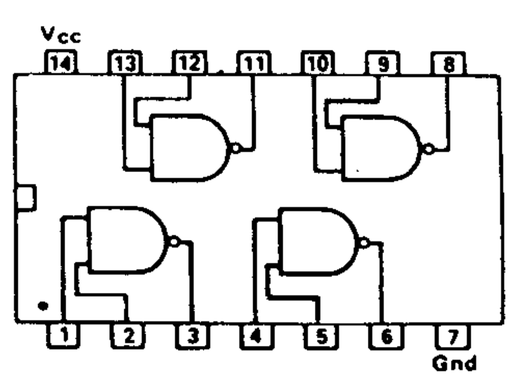
33 Quad 2-input NOR buffer-open collector outputs



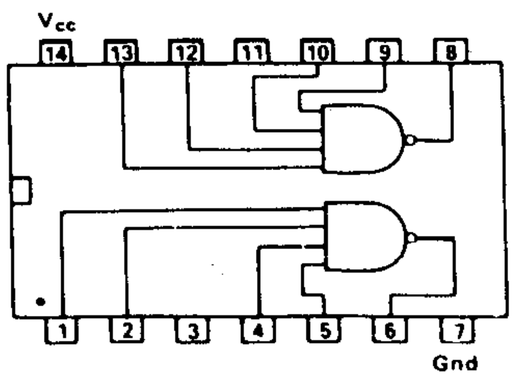
37 Quadruple 2-input NAND buffer



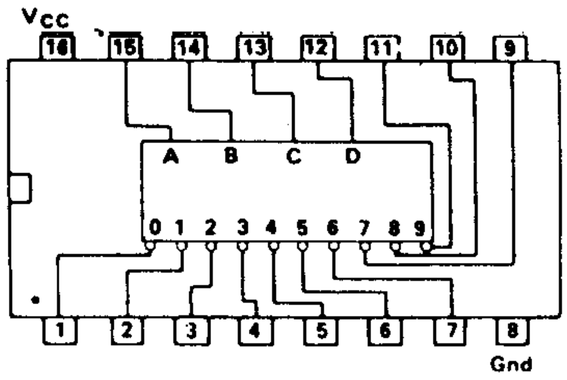
38 Quadruple 2-input NAND buffer – open collector outputs



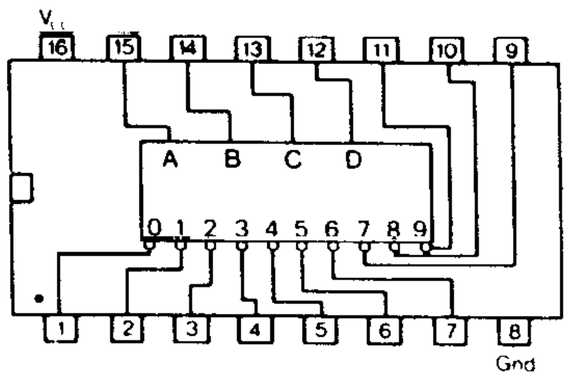
40 Dual 4-input NAND buffer



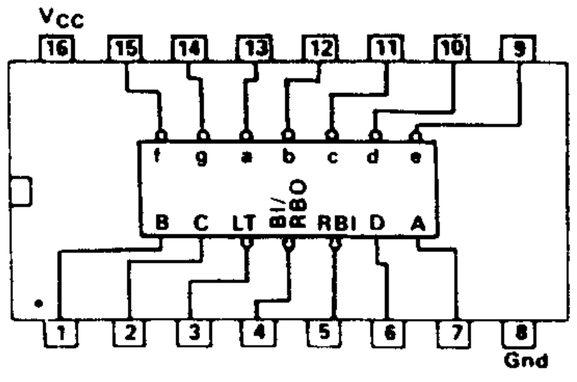
42 BCD-to-decimal decoder



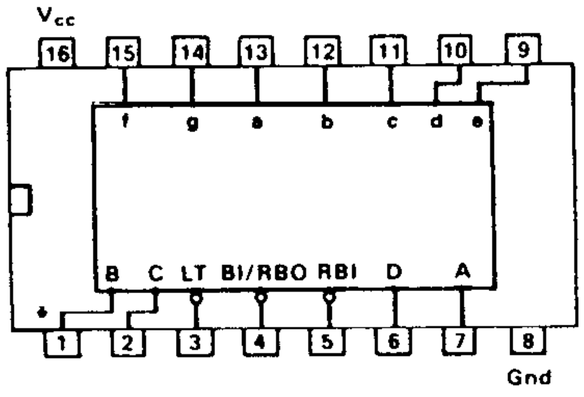
45 BCD-to decimal decoder/driver



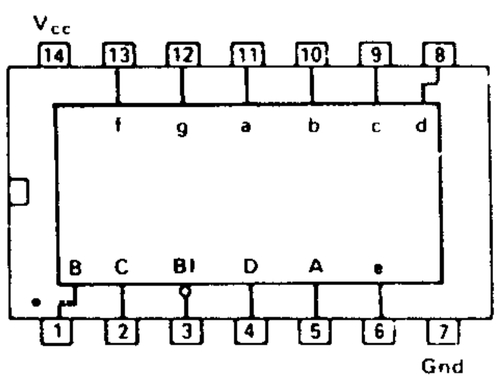
47 BCD-to-7 segment decoder/driver — open collector outputs



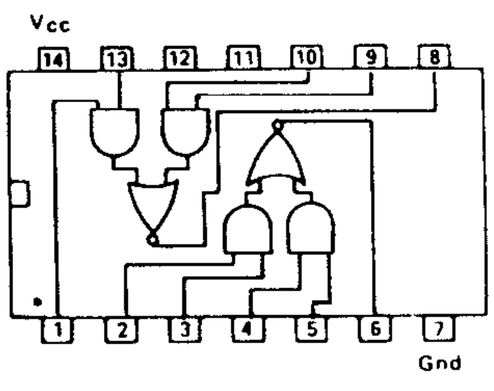
48 BCD-to-7 segment decoder/driver



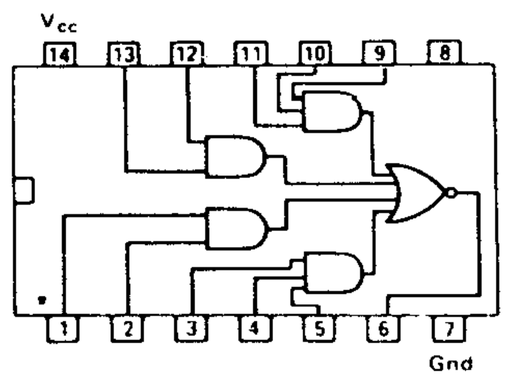
49 BCD-to-7-segment decoder/driver – open collector outputs



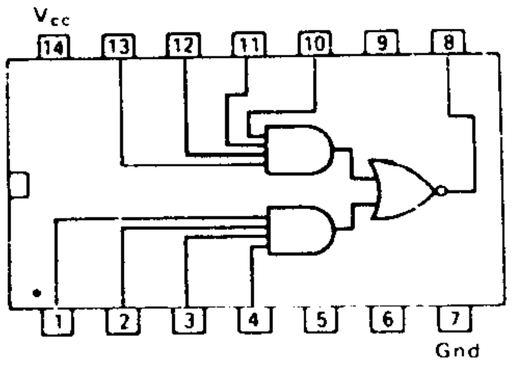
51 Dual 2-wide 2 input/3-input AND-OR-INVERT gate



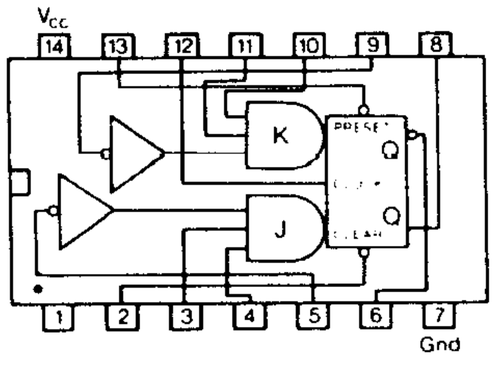
54 3-2-2-3 input AND-OR-INVERT gate



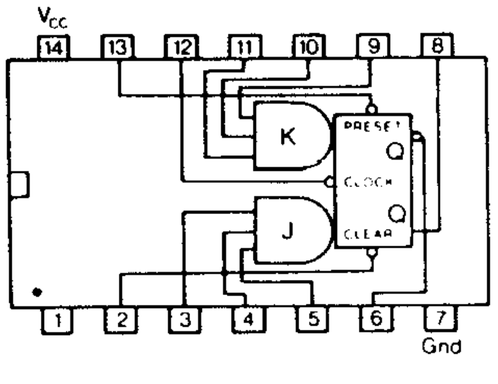
55 2-wide 4-input AND-OR-INVERT gate



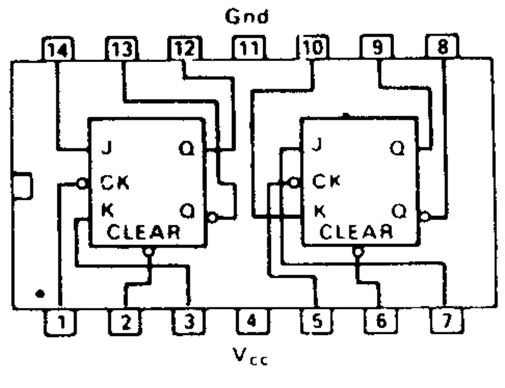
70 J-K flip-flop



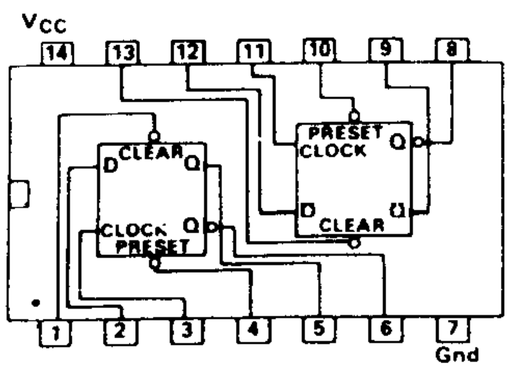
72 J-K master-slave flip-flop



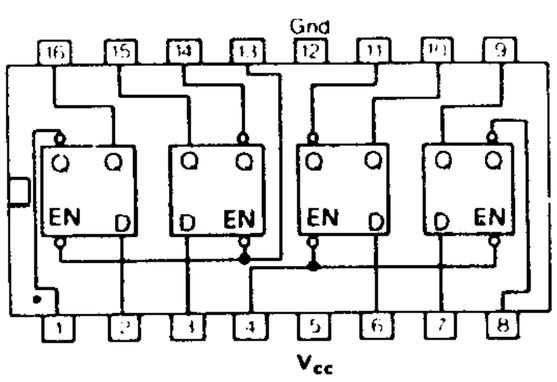
73 Dual JK negative edge-triggered Flip-Flop



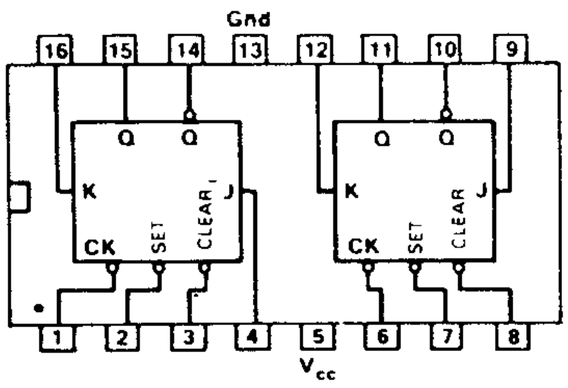
74 Dual D-type edge-triggered Flip-Flop



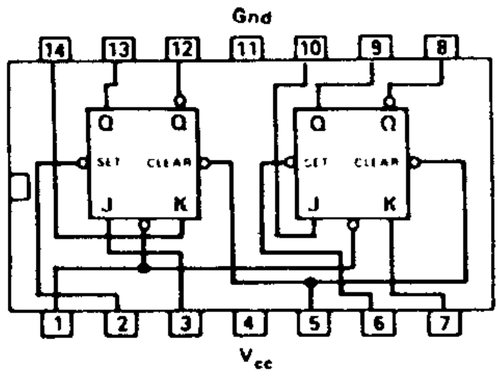
75 4-bit D Latch



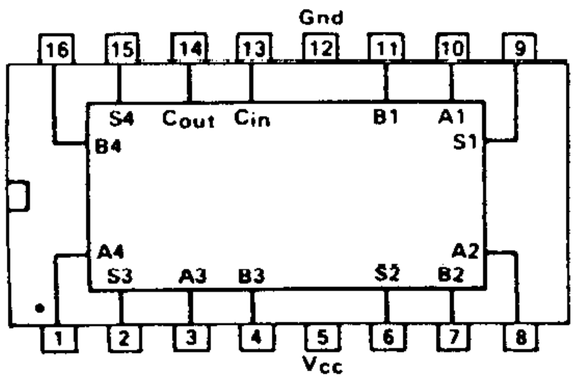
76 Dual JK Flip-Flop with set and clear



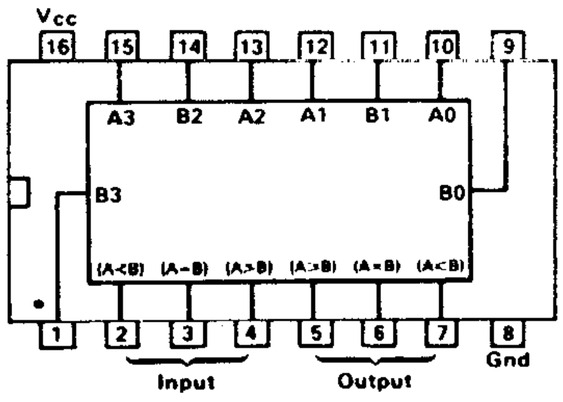
78 Dual JK Flip-Flop



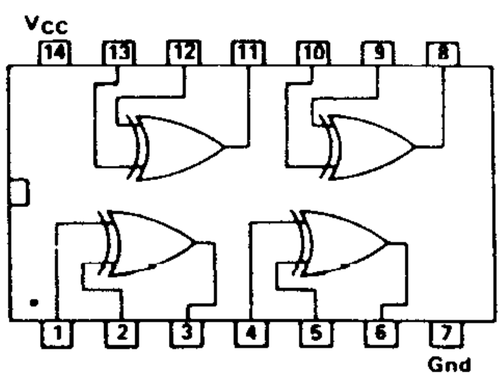
83A 4-bit Binary full adder



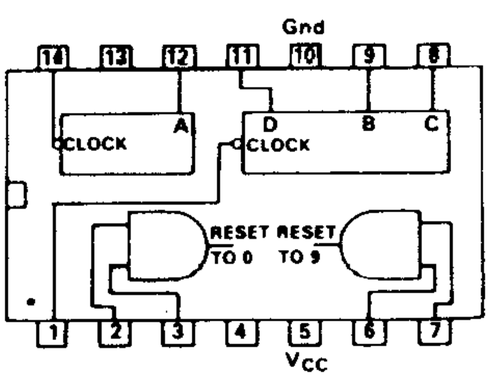
85 4-bit magnitude comparator



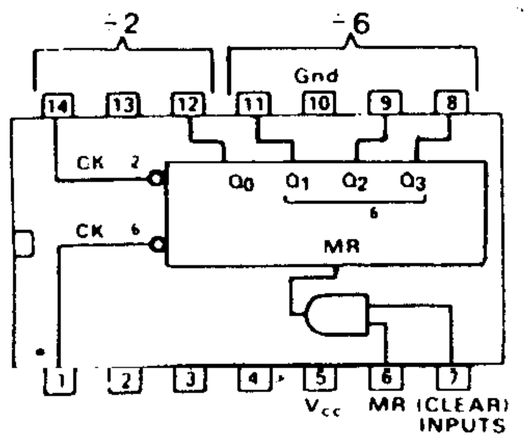
86 Quadruple 2-input exclusive OR gate



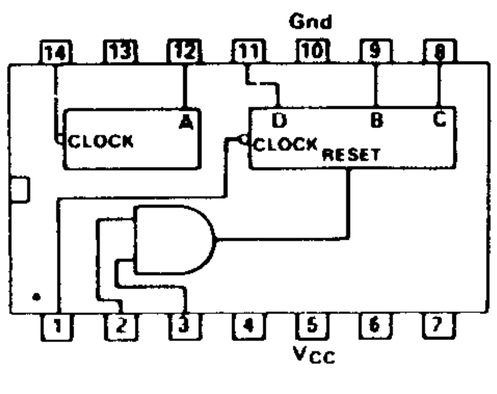
90 Decade counter



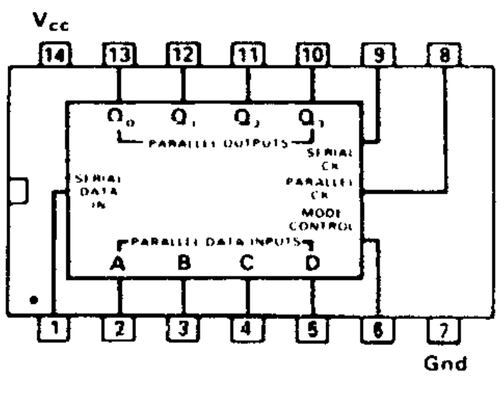
92 Divide-by-twelve counter



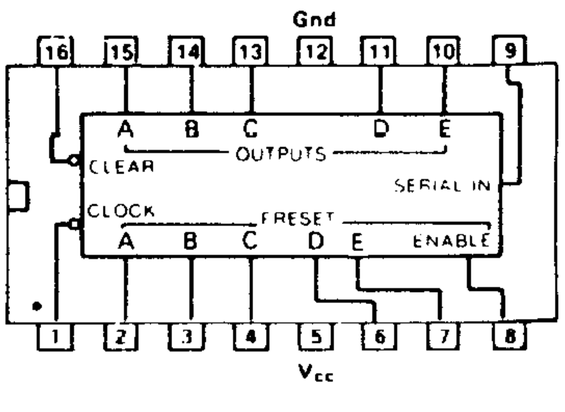
93 4-bit binary counter



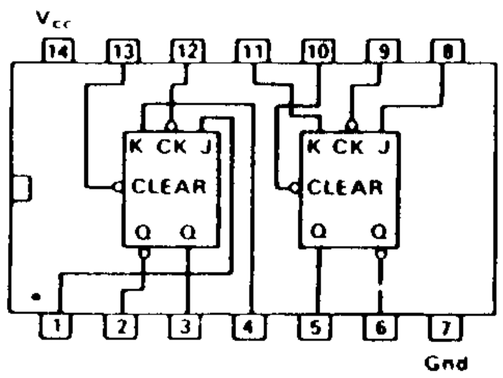
95B 4-bit shift register



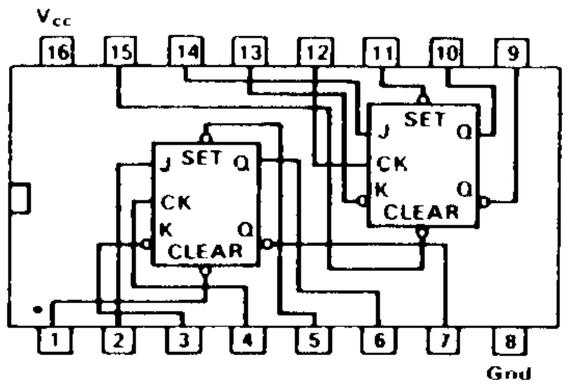
96 5-bit shift register



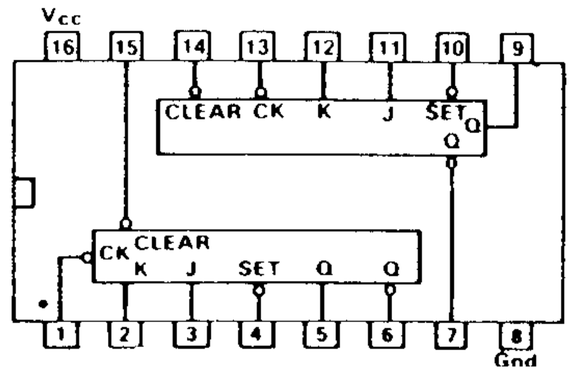
107 Dual JK Flip Flop



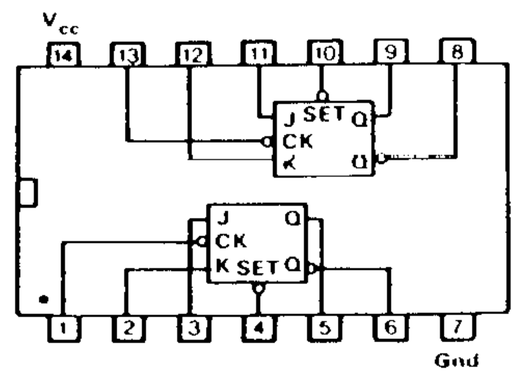
109 Dual JK positive edge triggered Flip Flop



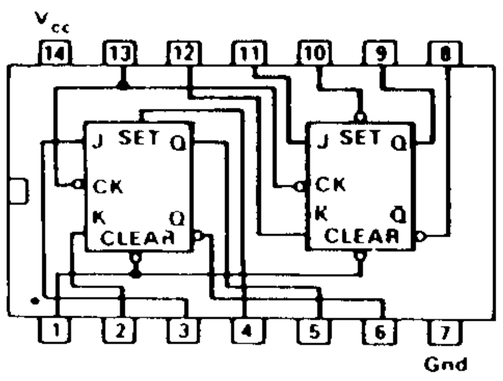
112 Dual JK edge triggered flip flop



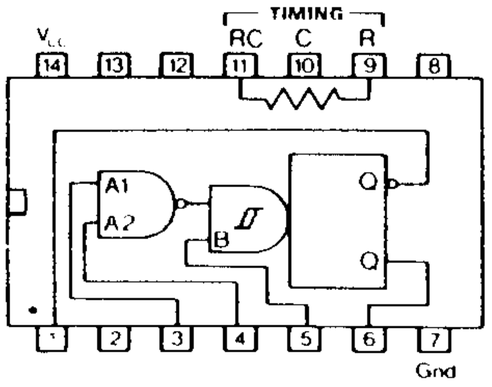
113 Dual JK negative edge triggered Flip Flop



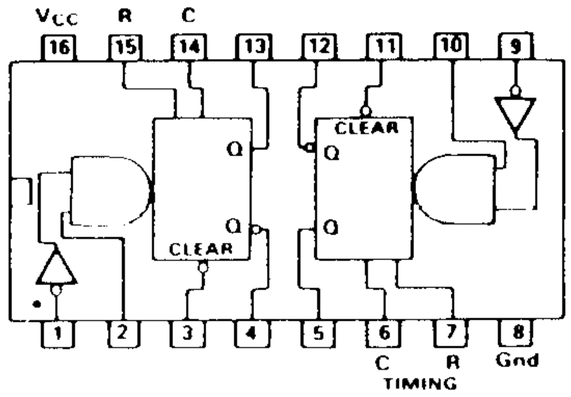
114 Dual JK negative edge-triggered Flip-Flop



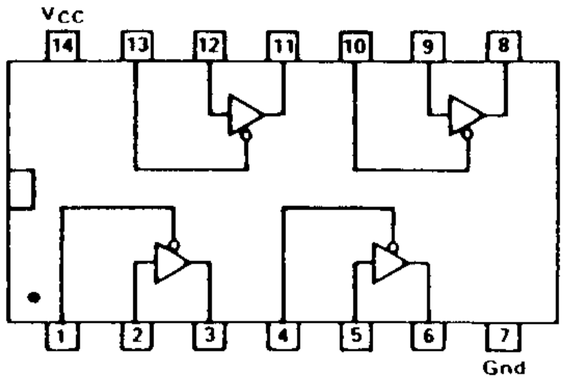
121 Monostable multivibrator



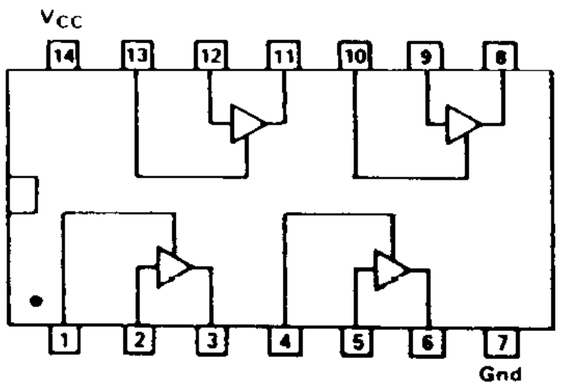
123 Dual monostable retriggerable



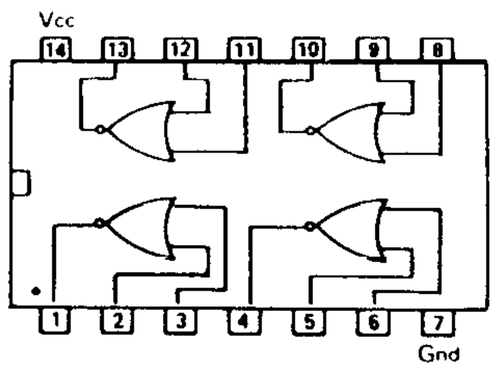
125 Quad 3-state buffer (active low enable)



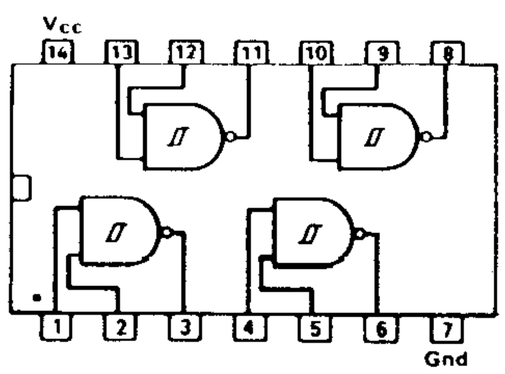
126 Quad 3-state buffer (active high enable)



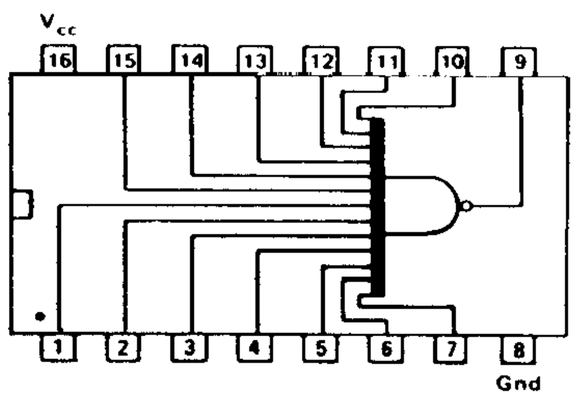
128 Quad line driver



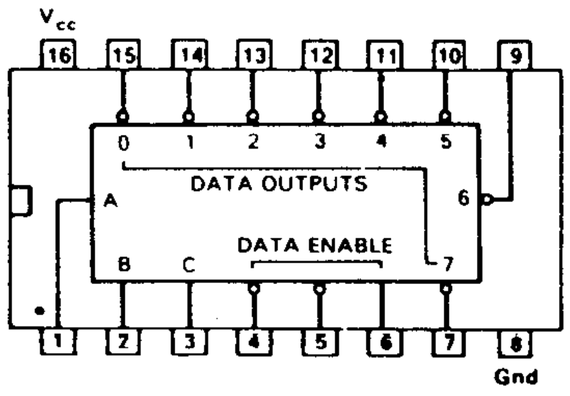
132 Quadruple 2-input NAND Schmitt gate



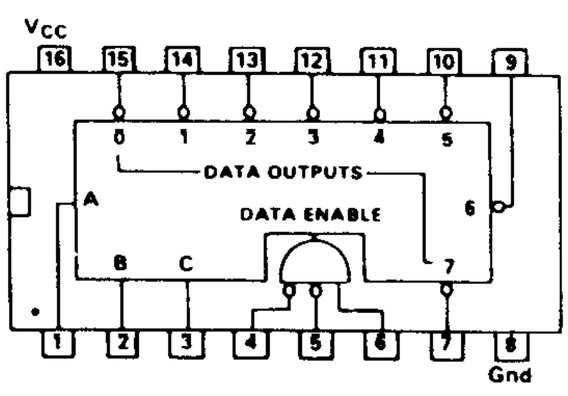
133 13-input NAND gate



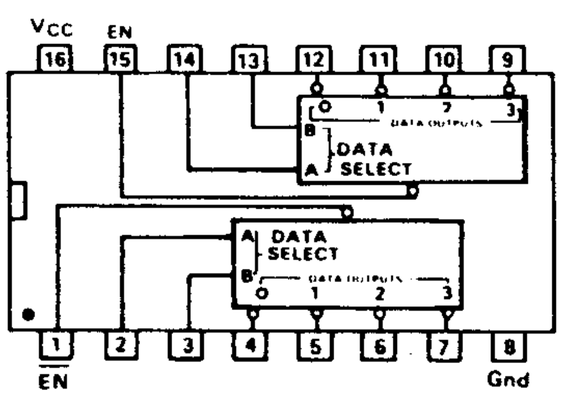
137 3-line to 8-line Decoder/Demultiplexer with address latches



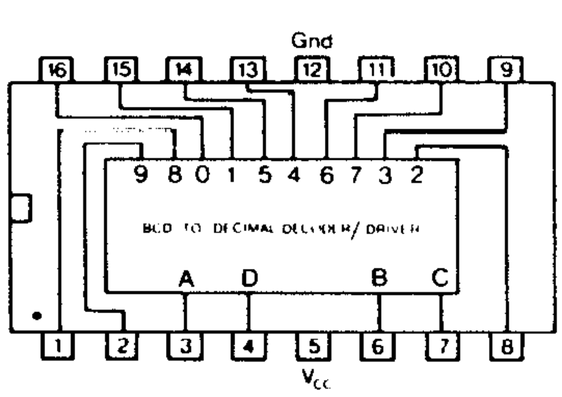
138 3 to 8 line Decoder/Multiplexer



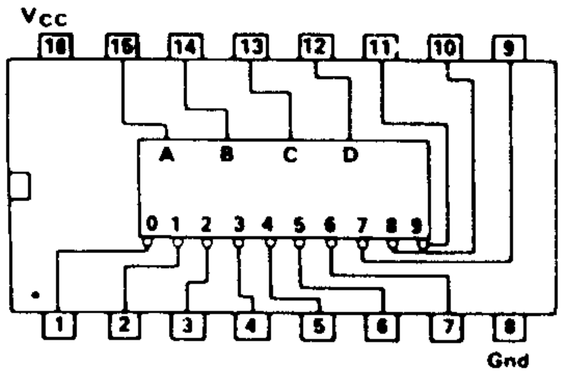
139 Dual 1 of 4 Decoder



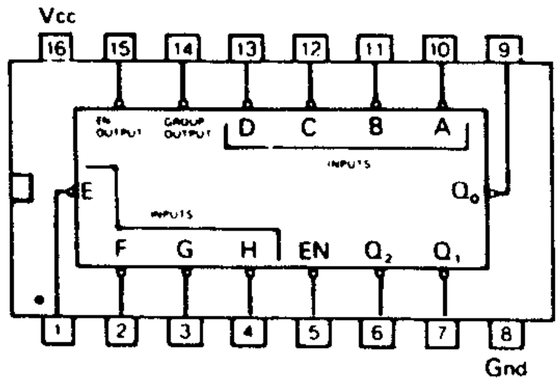
141 BCD to decimal decoder driver



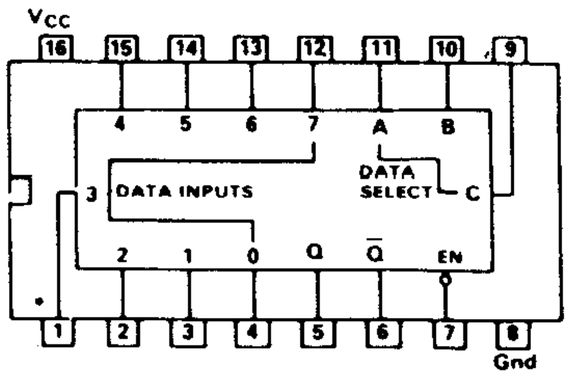
145 BCD-to-decimal decoder/driver



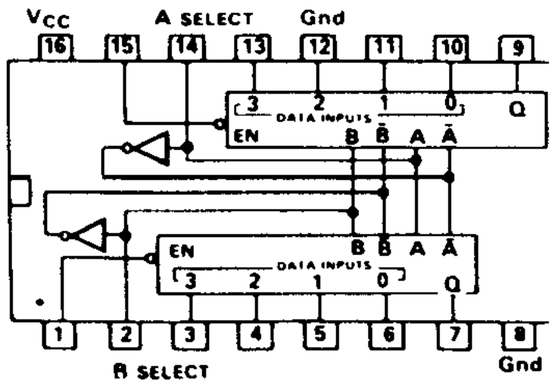
148 Octal priority encoder 8 line to 3 line



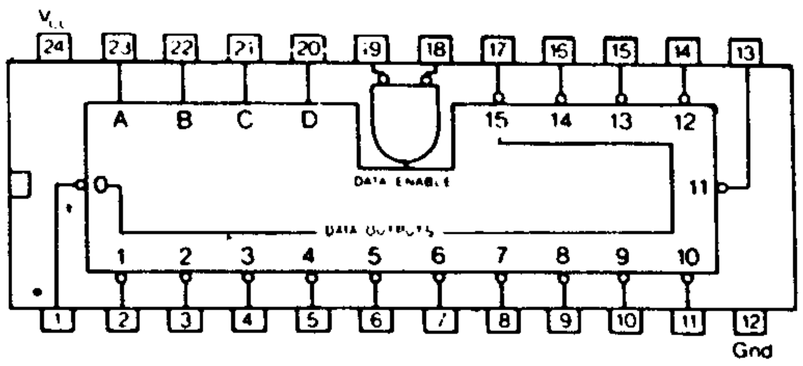
151 1 of 8 Data Selector/Multiplexer



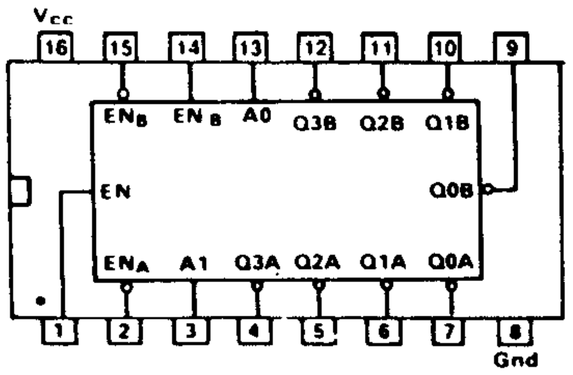
153 Dual 4-line to 1-line Data Selectors/Multiplexers



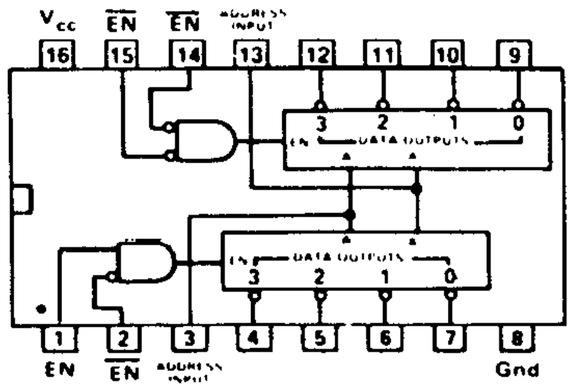
154 4 to 16 line Decoder



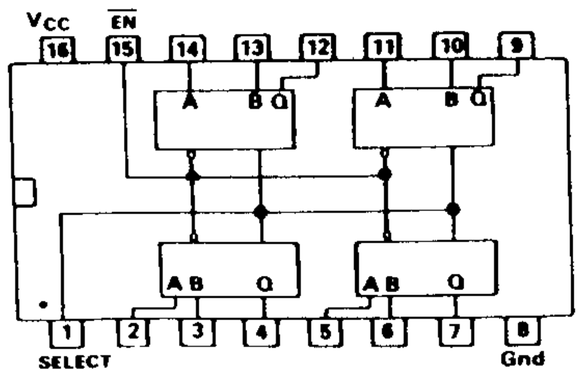
155 Dual 1 of 4 Decoder/Demultiplexer



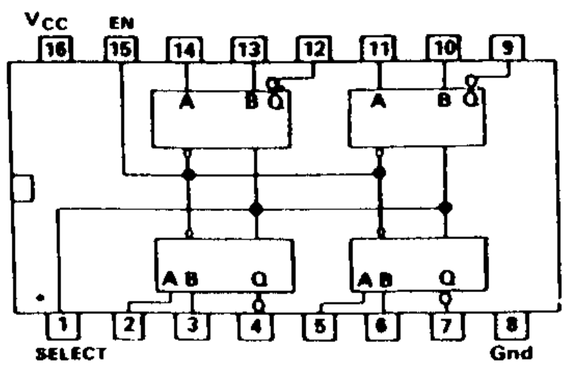
156 Dual 1-of-4 Decoder/Demultiplexer with open collector outputs



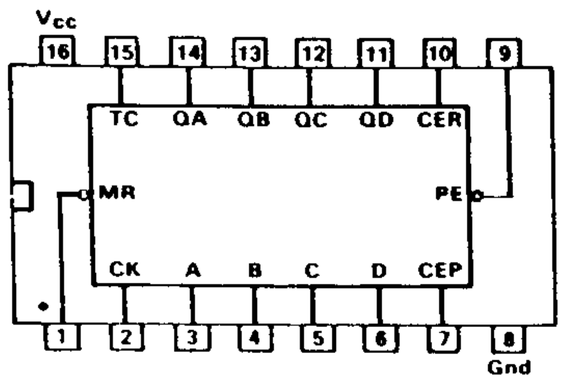
157 Quad 2 to 1-line Data Selectors / Multiplexers



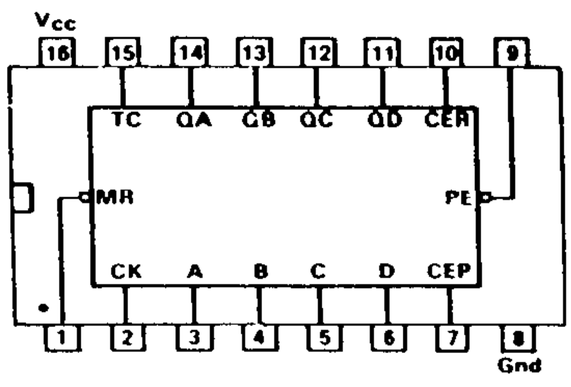
158 Quad 2 to 1-line Data selectors/Multiplexers with Inverted outputs



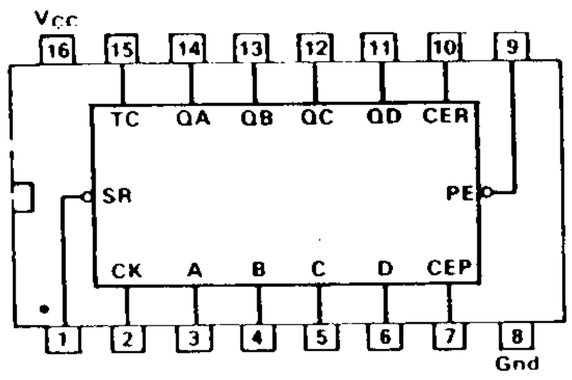
160 BCD decade counter — asynchronous reset



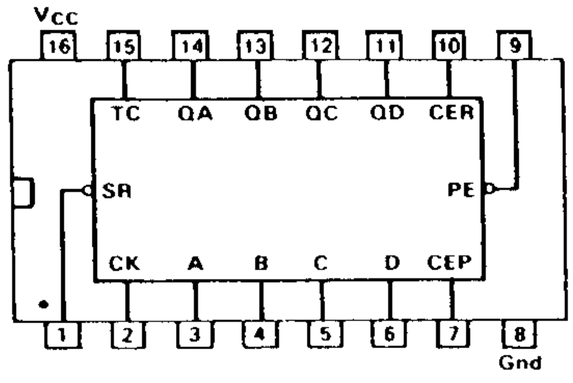
161 Binary counter — asynchronous reset



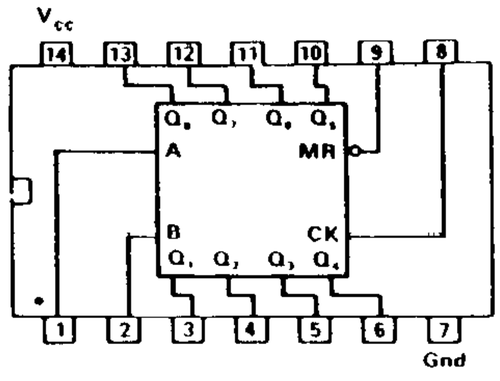
162 BCD counter — synchronous reset



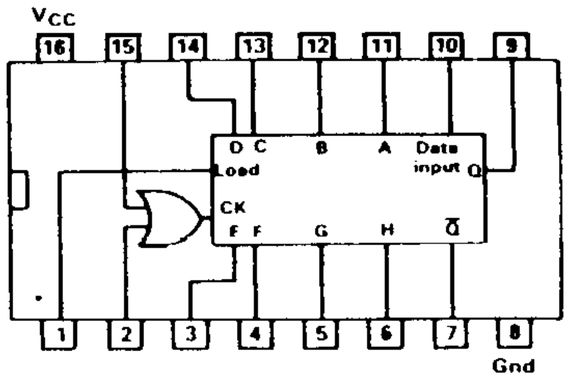
163 Binary counter — synchronous reset



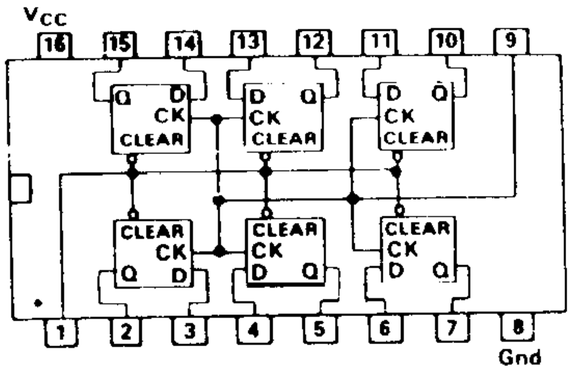
164 Serial-in parallel-out shift register



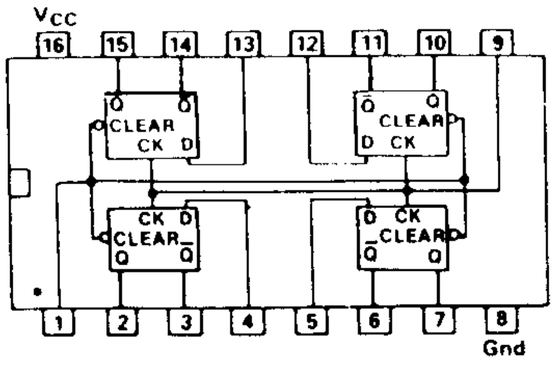
165 8-bit parallel to serial converter



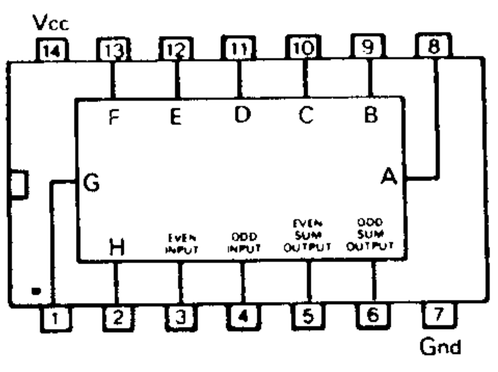
174 Hex D-type Flip-Flops



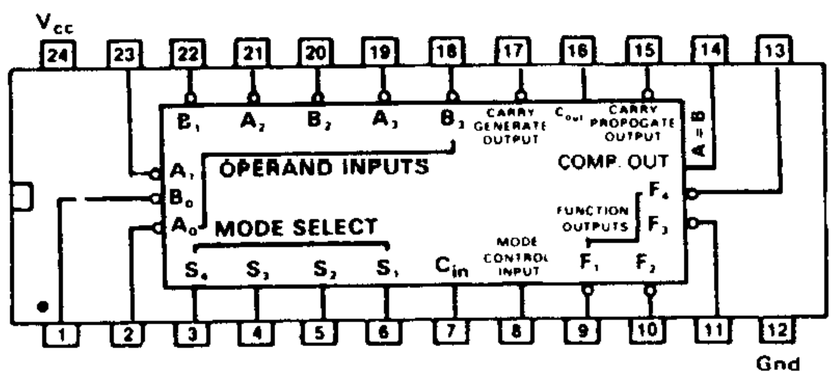
175 Quad D-type Flip-Flops



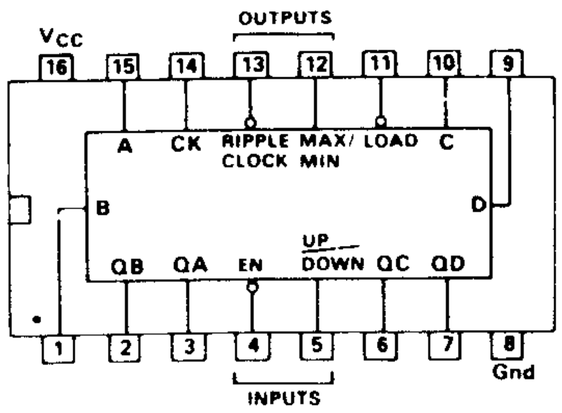
180 Parity generator/checker 9-bit odd/even



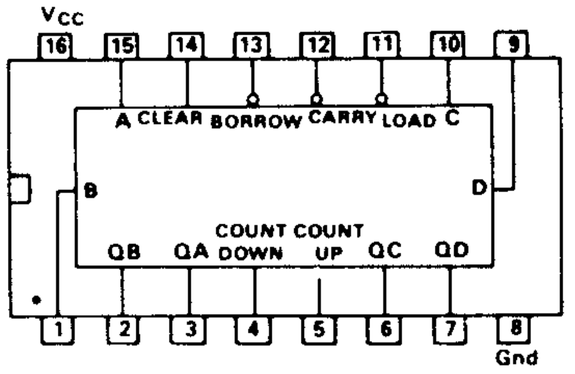
181 4-bit arithmetic logic unit



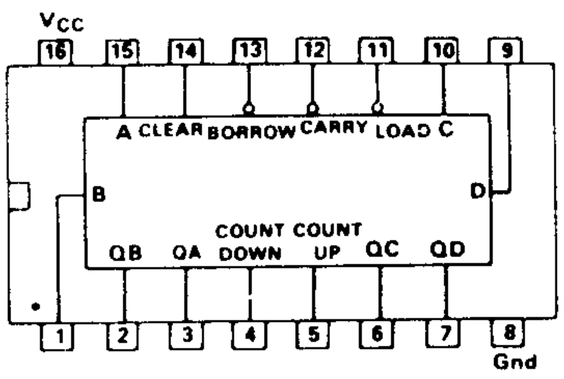
191 Binary synchronous up/down counter



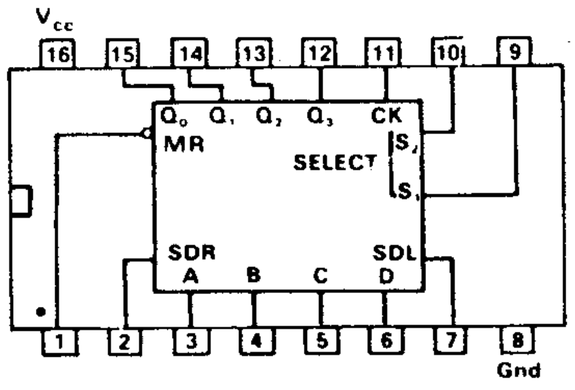
192 Up/Down decade counter — with preset inputs



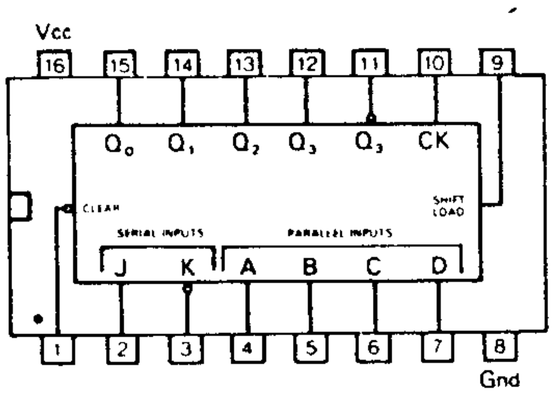
193 Up/Down binary counter-with preset inputs



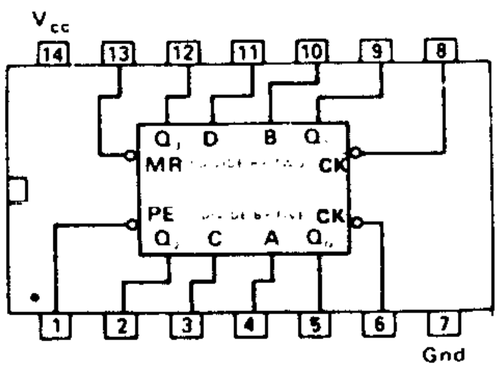
194 A 4-bit bidirectional universal shift register



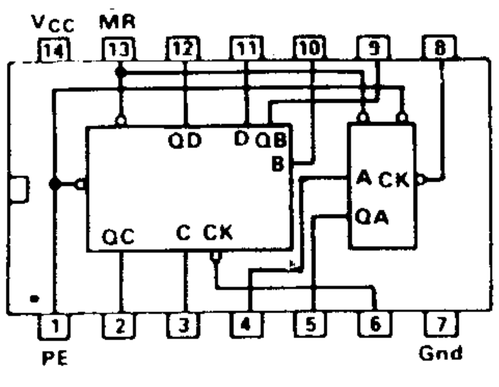
195 4-bit parallel-access shift register



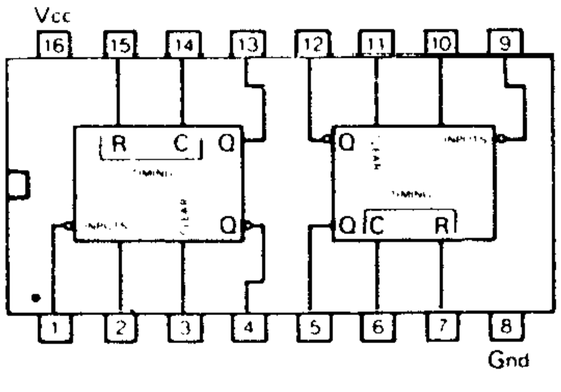
196 4-stage presettable ripple counter



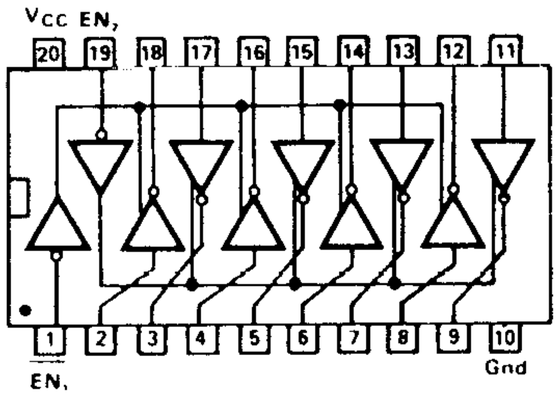
197 Presettable binary ripple counter



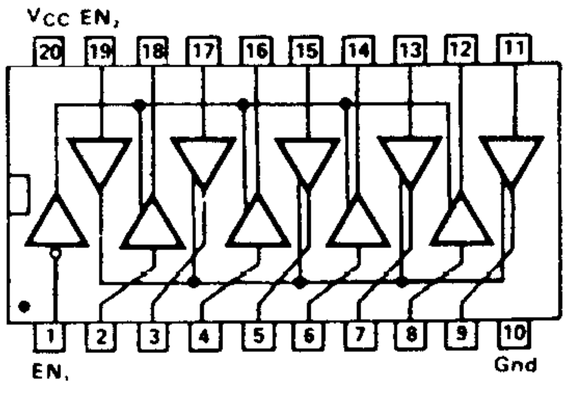
221 Dual monostable multivibrator



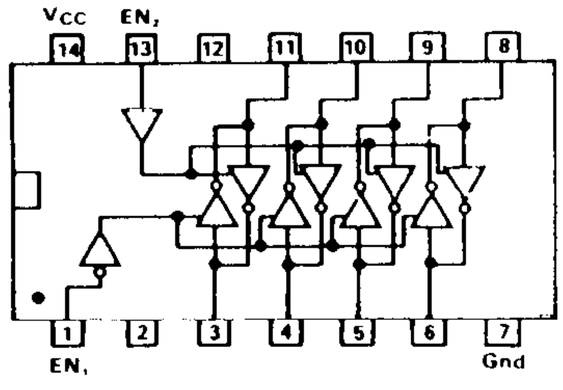
240 Octal buffer — three state inverting



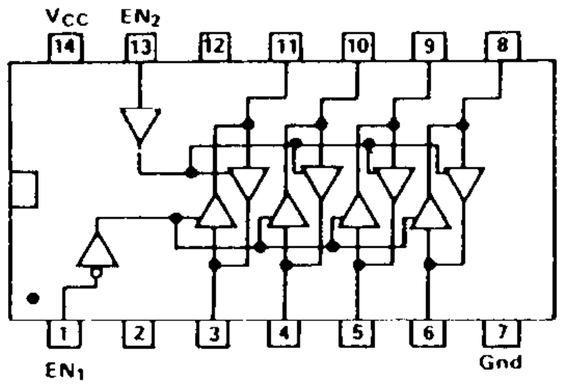
241 Octal buffer — three state non-inverting



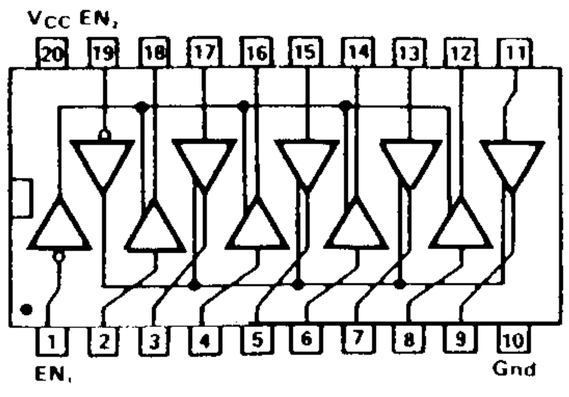
242 Quad bus transceiver inverting



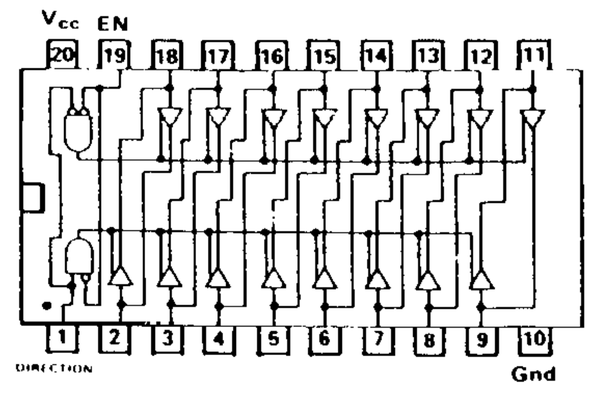
243 Quad bus transceiver - non-inverting



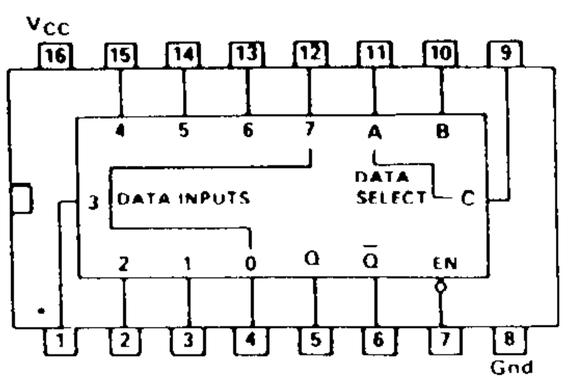
244 Octal buffer – three state non-inverting



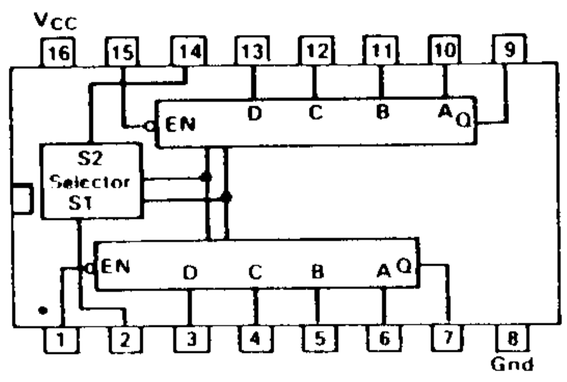
245 Octal bus transceiver with 3 state outputs



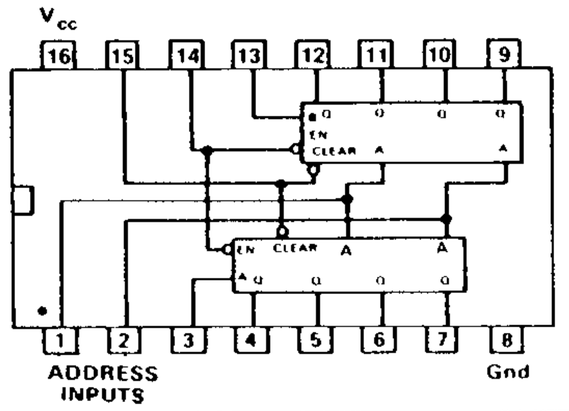
251 1 of 8 Data selector/Multiplexer with 3 state outputs



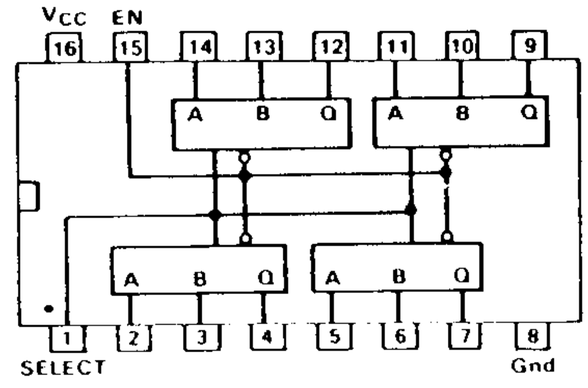
253 Dual 4 - input multiplexer with 3 state outputs



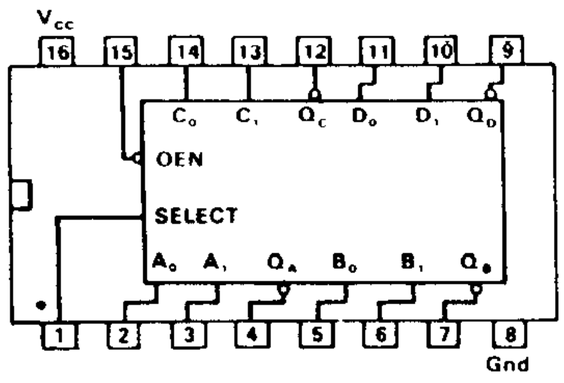
256 Dual 4-bit addressable latch



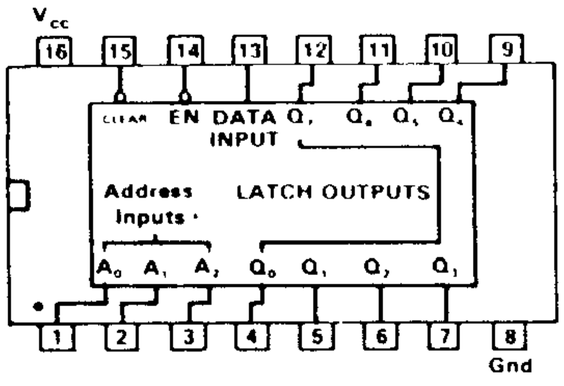
257 Quad 2-input multiplexer with 3 state outputs



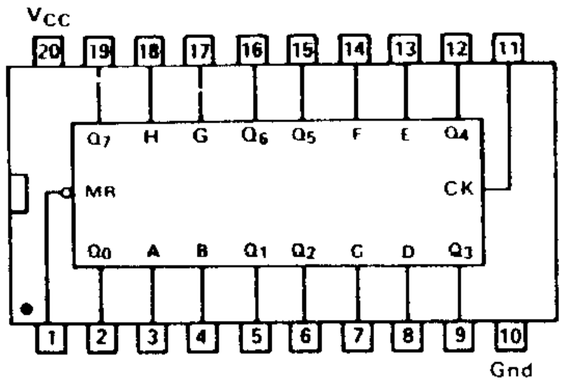
258 Quad 2-input multiplexer with 3 state outputs



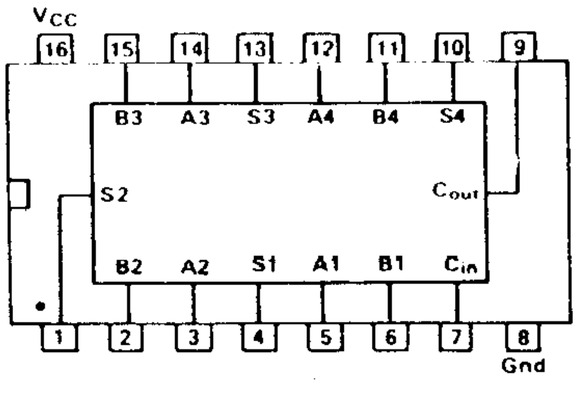
259 8 bit addressable latch



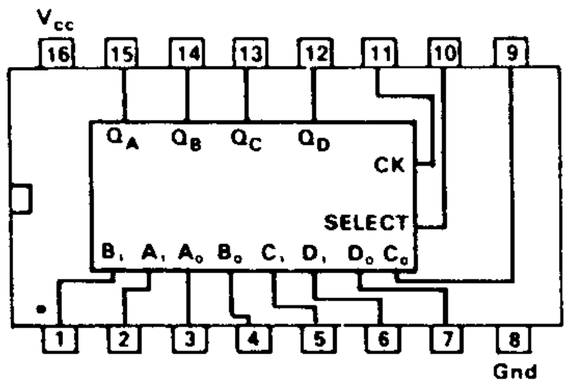
273 8-bit register with clear



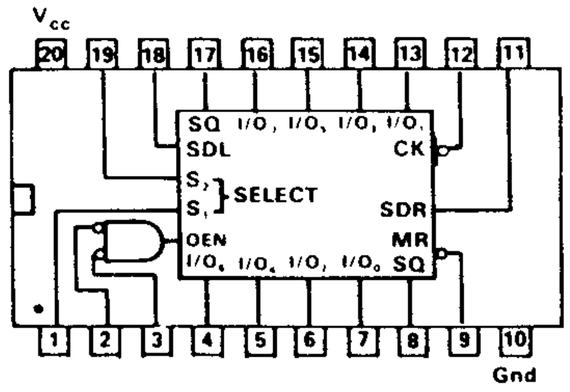
283 4 bit binary full adder



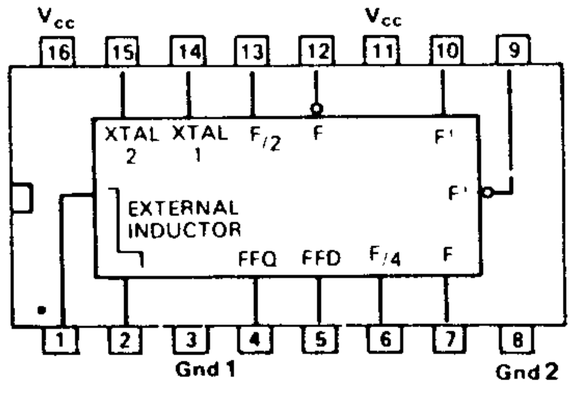
298 Quad 2-port register (Quad 2-input multiplexer with storage)



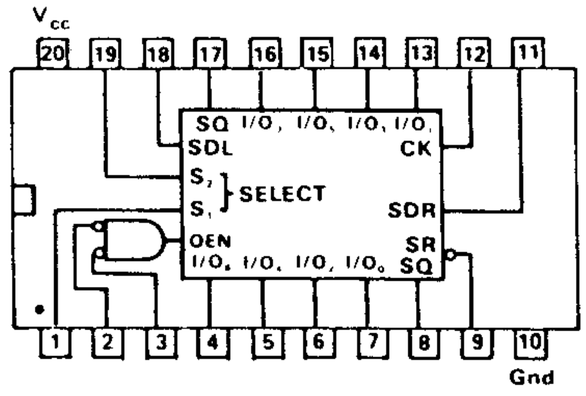
299 8-bit-universal shift /storage register with common parallel I/O pins 3 state



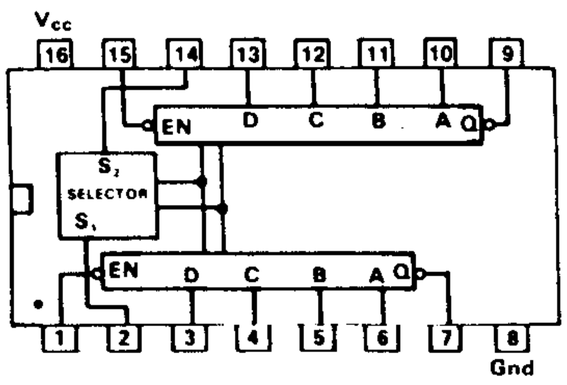
321 Crystal controlled oscillator



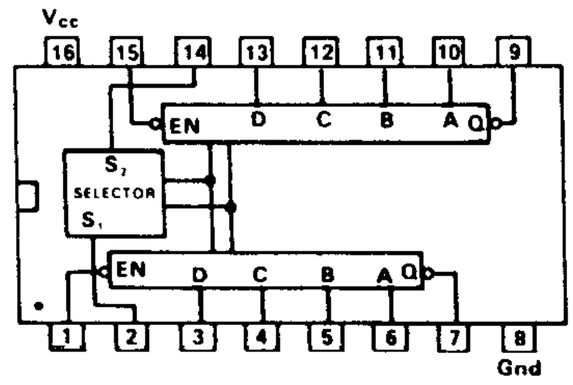
323 8-bit universal shift/storage register with synchronous reset and common I/O pins 3 state



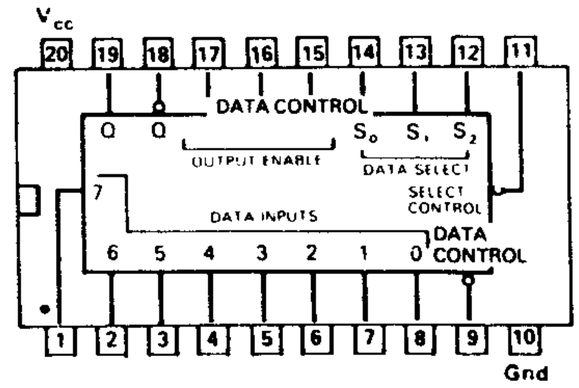
352 Dual 4-input multiplexer inverting



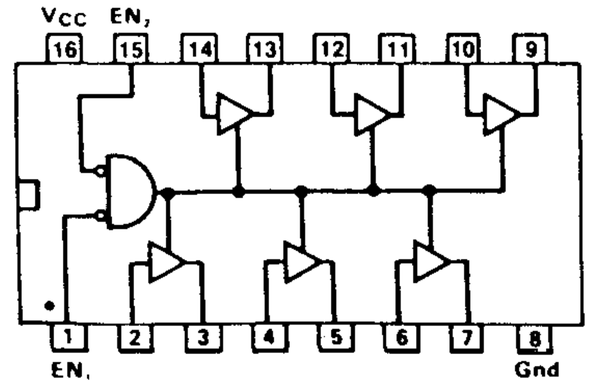
353 Dual 4-input multiplexer with 3 state outputs inverting



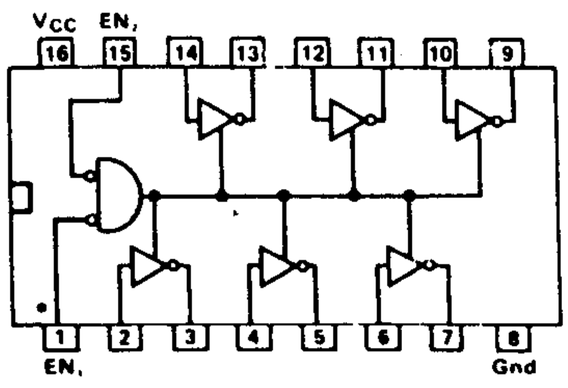
354/356 8-line to 1-line data selector/multiplexer/register



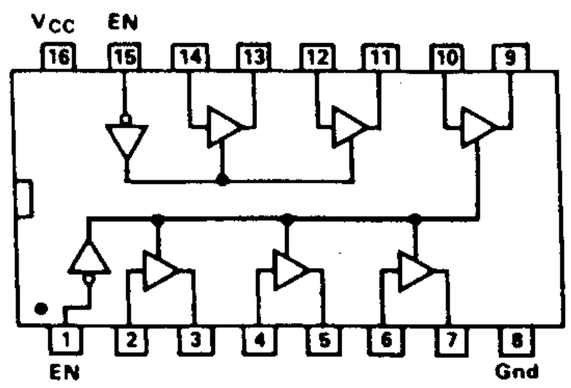
365 Hex 3 state buffer non-inverting



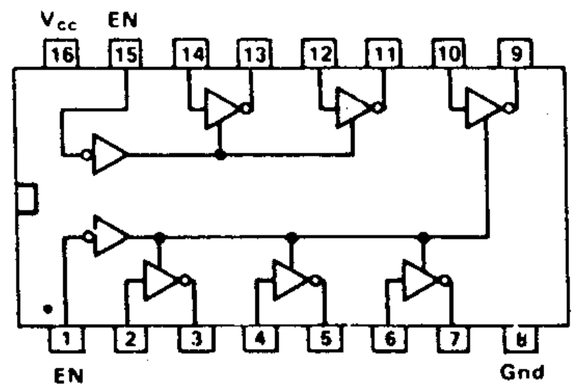
366 Hex 3 state buffer inverting



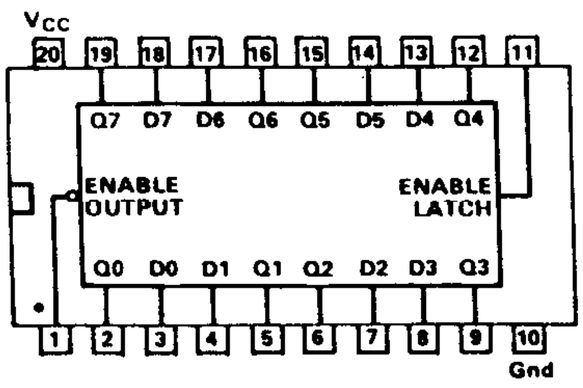
367 Hex 3-state buffer



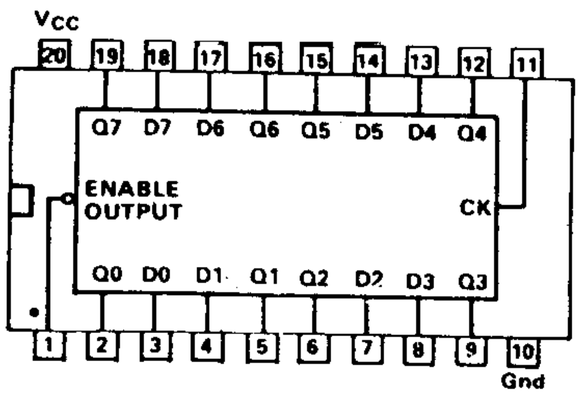
368 Hex 3-state inverter buffer (separate 2-bit & 4-bit sections)



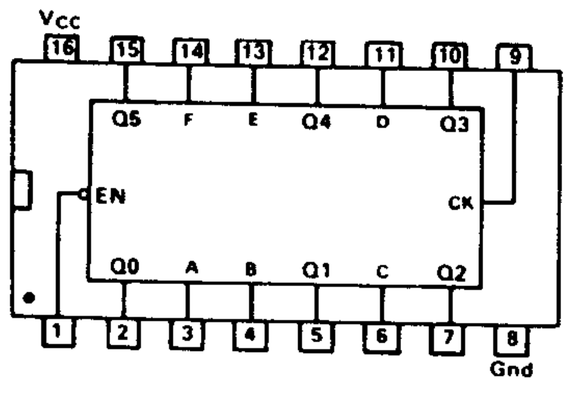
373 Octal transparent latch with 3 state outputs



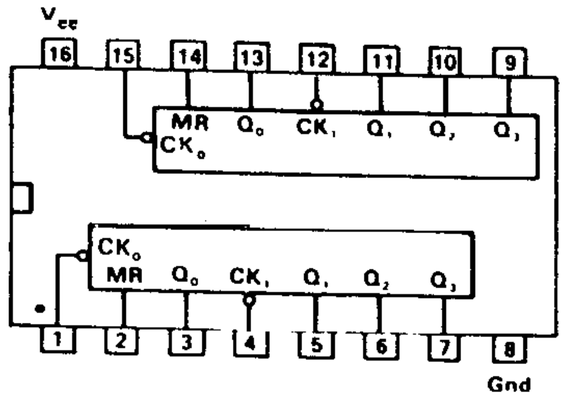
374 Octal D-type flip-flop with 3 state outputs



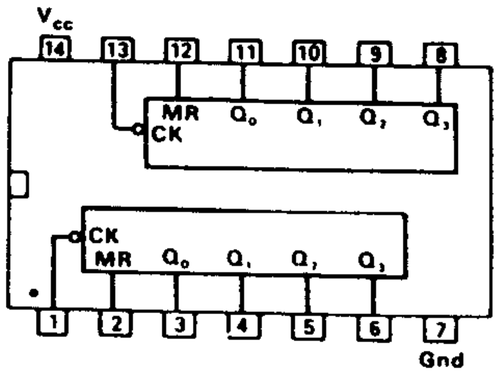
378 Hex D register



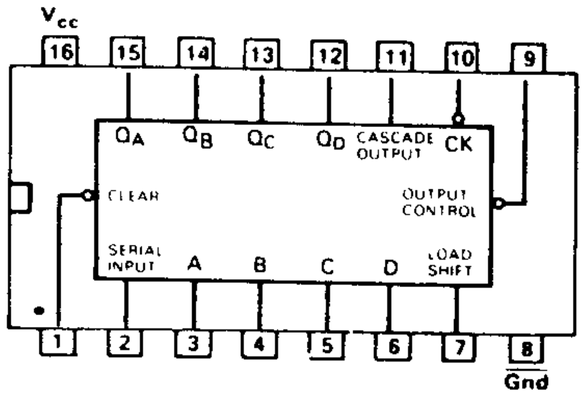
390 Dual decade counter



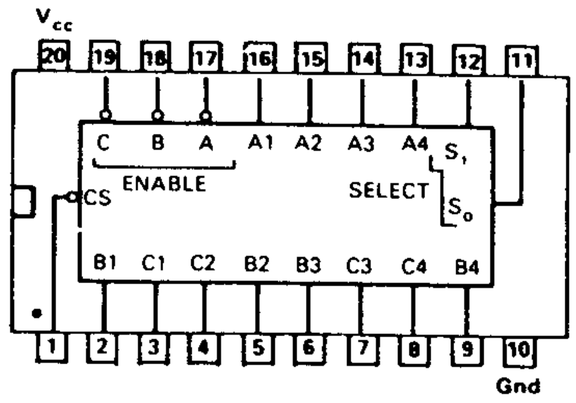
393 Dual 4 stage binary counter



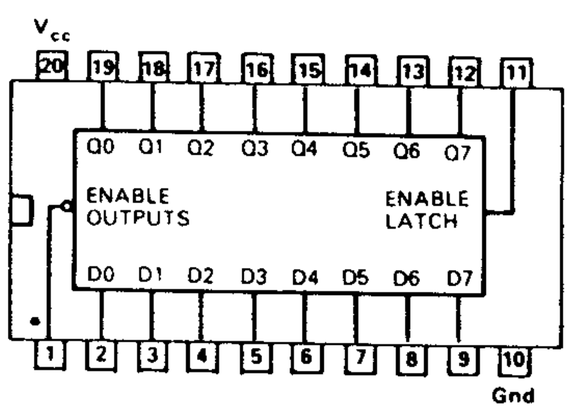
395 4-bit cascadable shift register 3 state



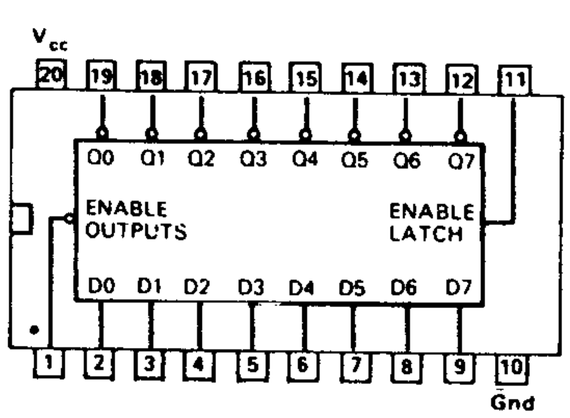
442, 443, 444 Quad tridirectional bus transceivers 3 state



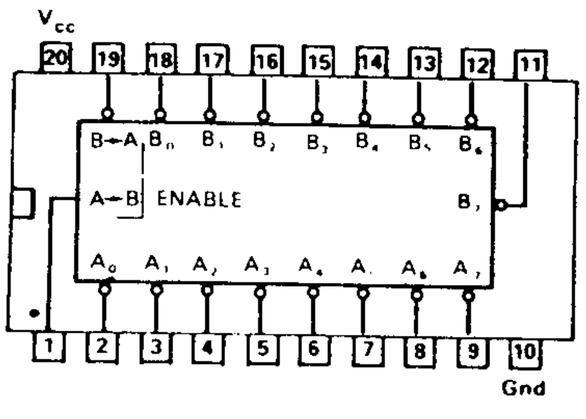
573 Octal D-type transparent latch



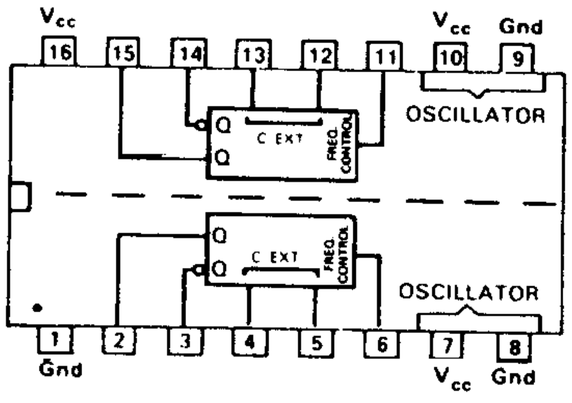
580 Octal D-type transparent latch inverted outputs



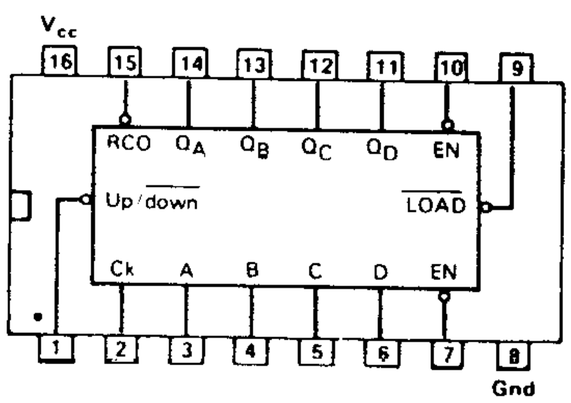
620 Octal bus transceiver



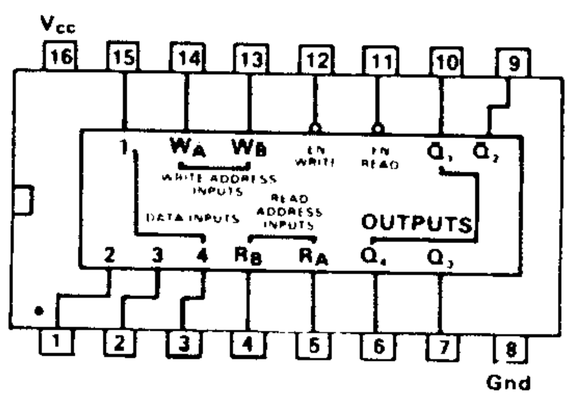
625 Voltage controlled oscillator



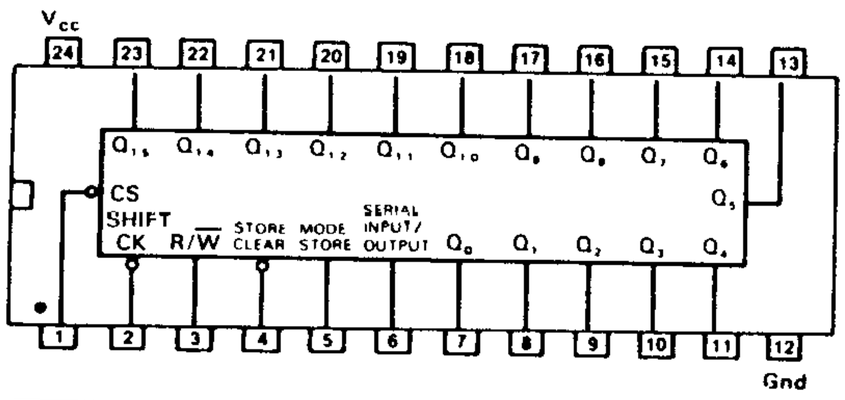
669 Up/down binary counter synchronous



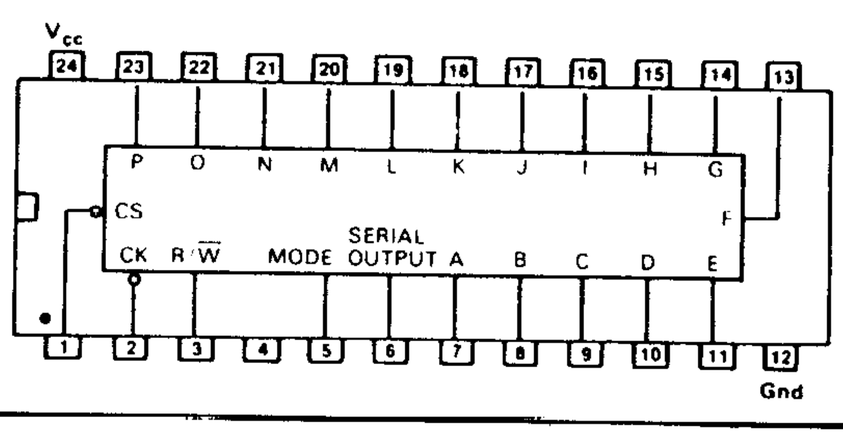
670 4 x 4 Register file with 3-state outputs



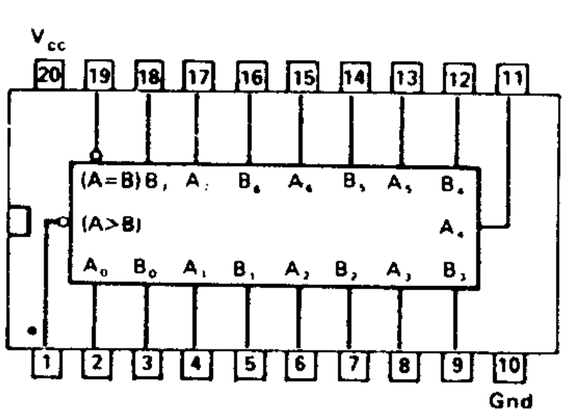
673 16-bit shift register, serial to parallel



674 16-bit shift register, parallel to serial



682 8-bit magnitude comparator



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